## REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Final Office Action dated July 10, 2006 has been received and its contents carefully reviewed.

Applicants thank the Examiner for courtesies extended during an interview with Applicants' representatives on October 12, 2006. The following remarks consider, in part, arguments discussed during the interview.

No claims are hereby amended; no claims are hereby canceled; no claims are hereby added. Accordingly, claims 1-32 are currently pending. Reexamination and reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 1-32 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 6,043,511 (to Kim)(hereinafter "Kim") in view of U.S. Patent Application Publication No. 2002/0117691 A1 (to Choi et al.)(hereinafter "Choi") and further in view of Applicants' Related Art (hereinafter "Related Art").

The rejection of claims 1-16 is respectfully traversed and reconsideration is requested. Claims 1-16 are allowable over the cited references in that each of these claims recite a combination of elements including, for example, "a gate electrode, a gate line and a gate pad electrode on a substrate, wherein all of the gate electrode, the gate line and the gate pad electrode have a double-layered structure including a first barrier metal layer and a first copper layer, wherein the first barrier metal layer is interposed between the substrate and the first copper layer and wherein the first barrier metal layer and the first copper layer have a smooth taper shape without any steps on their sides ... and a data line on the gate insulation layer crossing the gate line, source and drain electrodes contacting the ohmic contact layer, and a data pad electrode on the gate insulation layer, wherein all of the data line, the source and drain electrodes, and the data pad electrode have a double-layered structure including a second barrier metal layer and a second copper layer and wherein the second barrier metal layer is interposed between the substrate and the second copper layer ." None of the cited references including Kim, Choi and Related Art, singly or in any combination, teach or suggest at least these features of the claimed invention. Kim does not teach or suggest at least the feature of "a first barrier metal layer and a first copper

layer, wherein the first barrier metal layer is interposed between the substrate and the first copper layer." The Examiner recognizes that Kim does not teach or suggest at least this feature of the claimed invention. The Examiner then turns to Choi and states that, "it would have been obvious to one of ordinary skill in the art at the time of the invention was made ... for advantages such as to obtain low resistance wiring, as per the teachings of Choi." (Office Action at page 4). However, Applicants respectfully disagree. Any combination of Kim and Choi does not render obvious at least the noted claimed limitation because the structures of Kim and Choi are entirely different from Applicants' claimed invention. In Choi, the copper layer is a bottom-most layer and in direct contact with the substrate. Furthermore, neither Kim nor Choi teach or suggest at least, "all of the data line, the source and drain electrodes, and the data pad electrode have a double-layered structure including a second barrier metal layer and a second copper layer and wherein the second barrier metal layer is interposed between the substrate and the second copper layer." Accordingly, Applicants request that the Examiner reconsider the Examiner's rejection in view of Applicants arguments and remarks. Accordingly, claim 1 and claims 2-16, which depend either directly or indirectly on claim 1, are allowable over the cited references.

The rejection of claims 17-32 is respectfully traversed and reconsideration is requested. Claims 17-32 are allowable over the cited references in that each of these claims recite a combination of elements including, for example, "forming a gate electrode, a gate line and a gate pad electrode on a substrate, wherein all of the gate electrode, the gate line and the gate pad electrode have a double-layered structure including a first barrier metal layer and a first copper layer, wherein the barrier layer is interposed between the substrate and the first copper layer and wherein the first barrier metal layer and the first copper layer have a smooth taper shape without any steps on their sides; ... wherein all of the data line, the source and drain electrodes, the capacitor electrode and the data pad electrode have a double-layered structure including a second barrier metal layer and a second copper layer and wherein the second barrier metal layer is interposed between the substrate and the second copper layer." None of the cited references including Kim, Choi and Related Art, singly or in any combination, teach or suggest at least these features of the claimed invention. Applicants' arguments and remarks with respect to the rejection of claims 1-16 apply equally to the rejection of claims 17-32. Furthermore, Applicants note that in rejecting at least claim 17, the Examiner has not considered the limitation of the capacitor electrode but has stated, "[As] to claim 17, the method of forming the array substrate

for use in a liquid crystal display device merely recites the steps of forming each element and since each element must be formed to make the device, the method would have at least been obvious." (Office Action at page 5). Accordingly, Applicants request that the Examiner reconsider the Examiner's rejection and further consider the other limitations that the Examiner did not address. Accordingly, claim 17 and claims 18-32, which depend either directly or indirectly on claim 17, are allowable over the cited references.

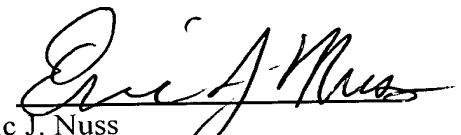
Thus, the Examiner is respectfully requested to consider the above remarks and to pass this application to issue.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: January 8, 2007

Respectfully submitted,

By 

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